AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

1-26 cancelled

27.(new) An electronic device comprising at least a memory core formed of an alloy serving as an electronic conductor and an electrode provided on each of both ends of the memory core, wherein

the memory core is formed of an alloy which can utilize the non-equilibrium state or the metastable state of a solid phase.

28.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is in a crystallographically stable state before writing or at the time of data recording and in which a non-equilibrium state accompanying with a solid-solid phase transition can be achieved during temperature increase.

29.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is in a crystallographically metastable state before writing or at the time of data recording and in which a non-equilibrium state accompanying with a solid-solid phase transition can be achieved during temperature increase.

30.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a compound before writing or at the time of data recording and which includes a component in which a phase transition to another crystal phase having the same composition takes place during temperature increase.

31.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a phase separated mixture before writing or at the time of data recording and in which a compound is generated during temperature increase.

32.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a supersaturated solid-solution before writing or at the time of data recording and in which phase separation takes place during temperature increase.

33.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a phase separated mixture before writing or at the time of data recording and in which the formation of a solid-solution takes place during temperature increase.

34.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a compound before writing or at the time of data recording and which includes a component in which phase separation can take

place during temperature increase.

35.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is an amorphous material before writing or at the time of data recording and in which crystallization takes place during temperature increase.

36.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a supersaturated solid-solution or a phase separated mixture before writing or at the time of data recording and in which spinodal decomposition or the formation of a solid-solution which is the inverse process can take place during temperature increase.

37.(new) The electronic device according to claim 27, wherein the memory core is formed of an alloy which is a compound or a phase separated mixture before writing or at the time of data recording and in which martensitic transformation can take place during temperature increase.

38.(new) The electronic device according to claim 27, wherein

at least one of the electrodes connected to the memory core is formed of a semiconductor also having a function for detecting junction resistance.

39.(new) The electronic device according to claim 27, comprising a third electrode directly connected to the memory

core or a third electrode positioned in close proximity of the memory core and insulated from the memory core, the third electrode for detecting a junction resistance, resistance, an electric potential, or an electric capacity.

40. (new) The electronic device according to claim 27, wherein

an interface between the memory core and the electrode directly connected with the memory core has a chemical potential adjusting layer having a thickness of at least 0.1 monolayers or more.

41. (new) The electronic device according to claim 27, wherein

the composition of the alloy forming the electronic device is caused to be biased by supplying an electric current to the electronic device to thereby write data on the electronic device.

42. (new) An integrated electronic device, wherein: a plurality of the electronic devices according to claim 27 are arranged in rows and columns; the electrode connected to one of both the ends of the memory core serves as a word line; the electrode selected from among the other electrodes of the memory core and directly provided on the memory core serves as at least a bit line; and writing-reading operation to the electronic device is achieved by selecting a word line and a bit line to access a certain electronic device of the

plurality of electronic devices arranged in rows and columns.

43. (new) An operation method for an electronic device comprising at least a memory core formed of an alloy serving as an electronic conductor and an electrode provided on each of both ends of the memory core,

wherein the memory core is formed of an alloy which can utilize the non-equilibrium state or the metastable state of a solid phase.

44. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is in a crystallographically stable state before writing or at the time of data recording, and the temperature of the memory core is changed such that the alloy is allowed to be in a non-equilibrium state accompanying with a solid-solid phase transition at the time of writing.

45. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is in a crystallographically metastable state before writing or at the time of data recording, and the temperature of the memory core is changed such that the alloy is allowed to be in a non-equilibrium state accompanying with a solid-solid phase transition at the time of writing.

46. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy having a component which is a compound before writing or

at the time of data recording, and the temperature of the memory core is changed such that a phase transition of the compound to another crystal phase having the same composition is allowed to take place at the time of writing.

47. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is a phase separated mixture before writing or at the time of data recording, and the temperature of the memory core is changed such that the phase separated mixture is allowed to generate a compound at the time of writing.

48. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is a supersaturated solid-solution before writing or at the time of data recording, and a temperature of the memory core is changed such that the supersaturated solid-solution is phase-separated at the time of writing.

49. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is a phase separated mixture before writing or at the time of data recording, and a temperature of the memory core is changed such that the phase separated mixture is allowed to form a solid-solution at the time of writing.

50. (new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy having a component which is a compound before writing or

at the time of data recording, and the temperature of the memory core is changed such that the compound is allowed to phase-separate at the time of writing.

51.(new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is an amorphous material before writing or at the time of data recording, and the temperature of the memory core is changed such that the amorphous material is allowed to crystallize at the time of writing.

52.(new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is a supersaturated solid-solution or a phase-separated mixture before writing or at the time of data recording, and the temperature of the memory core is changed such that the supersaturated solid-solution or the phase-separated mixture is allowed to spinodally-decompose or form a solid-solution which is the inverse process thereof at the time of writing.

53.(new) The operation method for an electronic device according to claim 43, wherein the memory core is formed of an alloy which is a compound or a phase separated mixture before writing or at the time of data recording, and the temperature of the memory core is changed such that martensitic transformation of the compound or the phase separated mixture is allowed to take place at the time of writing.

54.(new) The operation method according to claim 43, wherein

the composition of the alloy forming the electronic device is caused to be biased by supplying an electric current to the electronic device to thereby write data on the electronic device.